IN THE CLAIMS

Please amend the following claims 20, 26, 31, and 35, as indicated.

1.-19. (Cancelled)

20. (Currently amended) A method for aligning an instruction stream, the method comprising:

inputting an instruction stream into a second shifter, the instruction stream being obtained exclusively from a first shifter;

determining in a length decoder and in a first clock cycle, a length of a current instruction in the instruction stream;

if a successive instruction in the instruction stream is contained in ~~a first~~ the second shifter then shifting the instruction stream to a start of the successive instruction based exclusively on the length of the current instruction, said shifting being performed during the first clock cycle and within the ~~first~~second shifter; and

if the successive instruction is not contained in the ~~first~~second shifter then shifting the successive instruction into the ~~first~~second shifter from the ~~second~~first shifter in the same clock cycle and shifting the instruction stream to the start of the successive instruction one clock cycle later.

21. (Cancelled)

22. (Cancelled)

23. (Previously presented) The method of claim 20, wherein the second shifter is connected to the length decoder via a latch.

24. (Previously presented) The method of claim 20, wherein the first shifter is able to shift 8 bytes of data.

25. (Previously presented) The method of claim 20, wherein the first shifter is able to shift 16 bytes of data.

26. (Currently amended) A method for aligning instructions in an instruction stream, the method comprising:

determining a length of a first instruction in the instruction stream during a length decode stage; and

inputting the length of the first instruction to a two-stage instruction alignment stage comprising first and second shift operations performed by first and second shifters respectively, wherein an output of the first shifter exclusively defines data to be shifted by the second shifter, based exclusively on the length of the first instruction, and wherein an output of the second shift operation comprises instructions of the instruction stream aligned to a start of a successive instruction in the instruction stream immediately following the first instruction, the output of the second shift operation defining an input to the length decode stage, and wherein if the first instruction is contained in the second shifter said first instruction is shifted into a length decoder that performed the length decode stage in the same clock cycle in which the length of the first instruction was determined, and wherein if the first instruction is not contained in the second shifter, said first instruction is shifted from the first shifter one clock cycle later into the length decoder from the first shifter.

27. (Previously presented) The method of claim 26, wherein the first and second shifters are connected in series and are synchronized to the same clock cycle.

28. (Previously presented) The method of claim 27, wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes.

29. (Previously presented) The method of claim 26, wherein inputting the length of the first instruction comprises inputting said length directly from the length decoder to the second shifter.

30. (Previously presented) The method of claim 26, wherein inputting the length of the first instruction comprises inputting said length from the length decoder to the first shifter via an intermediate latch.

31. (Currently amended) Logic for aligning instruction in an instruction stream, the logic comprising:

a first shifter;

a second shifter; and

a length decoder, wherein an output of the first shifter forms a direct input to the second shifter and exclusively defines data to be shifted therein, an output of the second shifter is sent to the length decoder via an intermediate latch, and wherein a length of a current instruction in the length decoder is directly input into the second shifter and the second shifter shifts the data based exclusively on the length of the current instruction.

32. (Previously presented) The logic of claim 31, wherein a length of the current instruction in the length decoder is input into the first shifter via an intermediate latch.

33. (Previously presented) The logic of claim 31, wherein the first shifter has a greater shifting capacity than the second shifter.

34. (Previously presented) The logic of claim 31, wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes.

35. (Currently amended) Logic for aligning instructions in an instruction stream, the logic comprising:

first shifting means for shifting bytes of the instruction stream;

second shifting means for shifting bytes of the instruction stream; and

length decoding means for determining a length of an instruction in the instruction stream, wherein an output of the first shifting means forms a direct input to the second shifting means and exclusively defines data to be shifted therein, an output of the second shifting means is sent to the length decoding means via an intermediate latching means, and wherein a length of a current instruction in the length decoding means is directly input into the second shifting means and the second shifter shifts the data based exclusively on the length of the current instruction.

36. (Previously presented) The logic of claim 35, wherein a length of the current instruction in the length decoder means is input into the first second shifting means via an intermediate latch means.

37. (Previously presented) The logic of claim 35, wherein the first shifter means has a greater capacity than the second shifter means.